REMARKS

Reconsideration of the above-referenced application in view of the above amendment, and of the following remarks, is respectfully requested.

Claims 9-18 and 20-21 are pending in this case. Claim 21 is added herein and claims 1-8 are cancelled herein.

The Examiner rejected claims 9-12, 14, 15, 18 and 20 under 35 U.S.C.§ 103(a) as being unpatentable over Kent (U.S. Patent 6,130,016) in view of Krivokapic et al. (U.S. Patent 5,646,870).

Applicant respectfully submits that claim 9 is patentable over Kent in view of Krivokapic in view of Kent as there is no disclosure or suggestion in the references of visually inspecting the resist material for light and dark regions within the test pattern area, the light and dark regions representing a corresponding variance in the patterned feature area of the resist material. Instead, Krivokapic teaches actually measuring the CD's of the scribe line features and Kent teaches inspecting the pattern by checking the clarity of the pattern and comparing the size and shape of the test pattern to the size and shape of the pattern on the calibration reticle (col. 7 lines 30-35). Presumably, this is also done by actually measuring the pattern features, although how this is specifically accomplished is not discussed. Neither reference teaches or suggests visually inspecting the resist material for light and dark regions as required by the claim. Accordingly, Applicant respectfully submits that claim 9 and the claims dependent thereon are patentable over the references.

Applicant respectfully submits that claim 9 is further patentable over the references as there is no disclosure or suggestion in the references of a reticle layer having a test pattern area, wherein a portion of the test pattern area is within a step-distance of a portion of the patterned feature area, and patterning a resist material by

stepping the reticle, wherein the resist material as patterned by said reticle is used to form the feature of a semiconductor device after said visually inspecting. Kent teaches a test reticle having a test pattern to mimic a pitch of a semiconductor structure reticle. Kent does not teach using a reticle having a test pattern within a step-distance of a patterned feature area, wherein that reticle is used to pattern resist material to form the feature of the semiconductor device. Instead, Kent teaches a test reticle with only test patterns. A separate semiconductor structure reticle with the pattern feature area is used to form the features of the semiconductor device. Krivokapic teaches a test pattern and die area pattern on the same reticle. However, Krivokapic does not discuss the steps patterns (stage shifts) within the reticle (see, Instant Background, paragraph [0007]) and accordingly, does not discuss the location of the test pattern with respect to the feature patterns in terms of step patterns. Neither reference alone or in combination teaches using a reticle having a portion of the test pattern area within a step-distance of a portion of the patterned feature area, which is used to form the feature of a semiconductor device. Accordingly, Applicant respectfully submits that claim 9 is further patentable over the references.

The Examiner rejected claim 13 under 35 U.S.C.§ 103(a) as being unpatentable over Kent (U.S. Patent 6,130,016) in view of Krivokapic et al. (U.S. Patent 5,646,870), as applied to claim 12 above, and in further view of Ausschnitt et al. (U.S. Patent 5,914,784).

Applicant respectfully submits that claim 13 is patentable over Kent in view of Krivokapic and Ausschnitt for the same reasons discussed above relative to claim 9 from which claim 13 ultimately depends.

The Examiner rejected claims 16-17 under 35 U.S.C.§ 103(a) as being unpatentable over Kent (U.S. Patent 6,130,016) in view of Krivokapic et al. (U.S. Patent 5,646,870), as applied to claims 9-12 above, in view of Ausschnitt et al. (U.S. Patent 5,914,784).

Applicant respectfully submits that claims 16-17 are patentable over Kent in view of Krivokapic and Ausschnitt for the same reasons discussed above relative to claim 9 from which claim 16 and 17 ultimately depend.

Applicant respectfully submits that newly added claim 21 is patentable. Claim 21 requires, in a method of forming a semiconductor device, patterning a resist material using a reticle having a plurality of step areas within the reticle, wherein the reticle includes a patterned feature area corresponding to a desired feature of a semiconductor device and a test pattern area, wherein a portion of the test pattern area is within a step-area distance of a portion of said patterned feature area. The plurality of step-areas of the reticle are shown in Figure 1 (paragraph [0020]). Kent teaches a separate test reticles and semiconductor device reticles. Neither reference discusses step-areas within a reticle (versus stepping or scanning of the entire reticle in making duplicate devices on a wafer). Thus neither teaches using a reticle with multiple step-areas and having a test pattern area, wherein a portion of the test pattern area is within a step-area distance of a portion of the patterned feature area.

Claim 21 further recites visually inspecting the patterned resist material for light and dark regions, differences is the light and dark regions between the plurality of step areas representing a systematic variance in critical dimension (CD) in the patterned resist material. Krivokapic teaches actually measuring the CD's of the scribe line features and Kent teaches inspecting the pattern by checking the clarity of the pattern and comparing the size and shape of the test pattern to the size and shape of the pattern on the calibration reticle (col. 7 lines 30-35). Neither reference teaches or suggests visually inspecting the resist material for light and dark regions, much less wherein differences in the light and dark regions between the plurality of step areas represent a systematic variance in critical dimension (CD) in the patterned resist material, as required by the claim.

In light of the above, Applicant respectfully requests withdrawal of the Examiner's rejections and allowance of claims 9-18 and 20-21. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

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